High Capacity Prime Code Hierarchical Decoder with Delay Line Logic

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Abstract In this paper we propose a novel structure using multi-hierarchical modified prime code sequences for synchronous code division multiple access (S/CDMA) network to increase the capacity of decoder dramatically. By setting the threshold and optimal decision position(ODP), together with delay line logic we can discriminate the input codes correctly. This architecture improve the capacity of modified prime code hierarchical decoder from P^2 to 1362 $\times$ P^2 theoretically, with P being a prime number.

1. INTRODUCTION

Techniques of fiber-optic code division multiple access (CDMA), also called spread spectrum techniques, have been proposed by various authors recently[1]-[3]. Compared with asynchronous CDMA network, CDMA with frame synchronization (S/CDMA) require network access all users be synchronized in order to provide higher throughput and accommodation[4]. In such structures using modified prime code sequence as a spreading code for asynchronous CDMA or S/CDMA, there are only a few decoder capacity. In the Asynchronous CDMA system the number of subscribers is equal to P, and in the S/CDMA system the number of subscribers is equal to P^2 , where P is a prime. In this paper we propose a new approach to combine two distinct value of P of the modified prime code structures to form a new multi-hierarchical architecture to increase the capacity of decoder system.

2. SYSTEM DESCRIPTION

The system block diagram of hierarchical structure is shown in Fig. 1. We utilize different value of P of prime code sequence to implementation our architecture. Table 1, Table 2 show the modified prime code sequence for P = 3 = P_S and P = 7 = P_L, respectively. For example, a prime code sequence for P=7, $C_{6,0}$ in group 6 combines with P=3, $C_{0,1}$ in group 0, to form a two-layer hierarchical architecture. P=7, $C_{6,0}$ in group 6 consists of seven delay lines: 1L, 14L, 20L, 26L, 32L, 38L, 44L ,and P=3, $C_{0,0}$ in group 0 consists of three delay lines: 3L, 6L, 9L. At the receiver end, the decoder collects the time-shifted pulses from each path of the tapped delay lines and sum up the time-shifted pulses. The receiver output *r(n)* is define as follow[5]

$$r(n) = \sum_{k=1}^{N} s(k) f(n-k) \qquad (1)$$

If the incoming signal has arrived at the correct destination, then $s(n)=f(n)$, and (1) represents an autocorrelation function; otherwise it represents a cross-correlation function. Through the optimal decision position(ODP) and delay line logic(DLL) together, the decoder will produce a peak amplitude, thus we can discriminate the input codes correctly. This novel system can improve the capacity from $P_L{}^2$(modified prime codes) to 1362 $\times$ $P_L{}^2$(multi-hierarchical prime code decoder) theoretically. There are still some failure groups exist in the theoretical capacity after simulations, however.

3. ANALYSIS

At the receiver end, if the signal arrived at the correct destination, then we get the autocorrelation function, otherwise, we get the cross-correlation function. It is necessary to maximize the autocorrelation function and minimize the cross-correlation function to optimize the system performance[5]. The signature sequences suited in previous studied[2],[3], and the possible code for the S/CDMA is the modified prime code sequence[4]. In such a code sequence the length of a certain signature sequence is equal to P^2. We combine two different value of P(P_L : Larger value of P, and P_S : Smaller value of P)value of modified prime code sequence to form a multi-hierarchical prime code sequences, and Fig. 2 shows the critical process of combination. By replacing the specific bit 0 portion in certain of larger of P=P_L value among the modified prime code sequence to all group in smaller of P=P_S value among the modified prime code sequence. Thus in each operation we can get an additional $P_S{}^2$ codes if we use the two-layer structure, and an additional $P_S{}^2 \times P_S{}^2$codes if we use the three-layer structure, and an additional $P_S{}^2 \times P_S{}^2 \times P_S{}^2$ codes for the four-layer structure. Fig. 2 also list the additional codes in two-layer structure, and Fig. 3 list the additional codes in three-layer structure. From this point of view we know that the more the layer numbers are , the more the codes exist. Finally we use an optimal decision position(ODP) with delay line logic(DLL) to discriminate the interferers, as shown in Fig. 4. Fig. 4(a) shows an example of the autocorrelation function from one group of the modified prime code sequences without combination. Fig. 4(b) shows the autocorrelation function with combination. If the amplitude in Fig. 4(b) is greater than the cross-correlation amplitude in Fig. 4(c), then the decoder can work at certain values of ODPs and DLL. We propose the algorithm for designing the multi-hierarchical prime code architecture and find the optimal decision position (ODP) for the decoder as shown in Table III.

4. SYSTEM CAPACITY

Total theoretical capacity of the novel architecture with the combination for $P_L = P_7 = 7$ and $P_S = P_3 = 3$ is calculated in the following sections.

4.1 Parameter Definition

In order to simplify our calculation process, we define some parameters below :

S_m : The total numbers of equip consecutive m '0' between adjacent 1.

$S_{m-(n)}$: The total numbers of equip consecutive m '0' between adjacent 1, and there are n portion equip m '0' in the certain sequence.

S_m : $S_m = \sum_{n} S_{m-(n)}$

S_{12} : The total numbers of equip consecutive 12 '0' between adjacent 1.

$S_{11-(1)}$: The total numbers of equip consecutive 11 '0' between adjacent 1, and there are only one portion equip 11 '0' in the certain sequence.

$S_{11-(2)}$: The total numbers of equip consecutive 11 '0' between adjacent 1, and there are two portion equip 11 '0' in the certain sequence.

$S_{11} = S_{11-(1)} + S_{11-(2)}$

$S_{10-(2)}$: The total numbers of equip consecutive 10 '0' between adjacent 1, and there are two portion equip 10 '0' in the certain sequence.

$S_{10-(3)}$: The total numbers of equip consecutive 10 '0' between adjacent 1, and there are three portion equip 10 '0' in the certain sequence.

$S_{10} = S_{10-(2)} + S_{10-(3)}$

$S_{9-(3)}$: The total numbers of equip consecutive 9 '0' between adjacent 1, and there are three portion equip 9 '0' in the certain sequence.

$S_{9-(4)}$: The total numbers of equip consecutive 9 '0' between adjacent 1, and there are four portion equip 9 '0' in the certain sequence.

$S_9 = S_{9-(3)} + S_{9-(4)}$

4.2 Two Layer

Two-layer structure in prime number equal to 7 exist only in group 3,4,5 and 6. Fig. 2 shows an instance of the case. System capacity belong to the case is calculated as follow :

$$C_{\text{Two Layer}} = (S_{12}\times 4 + S_{11}\times 3 + S_{10}\times 2 + S_9\times 1)\times P_3^2 = 1080$$

where $S_{12} = 6$;
$S_{11} = S_{11-(1)} + S_{11-(2)} = 12$;
$S_{10} = S_{10-(2)} + S_{10-(3)} = 18$;
$S_9 = S_{9-(3)} + S_{9-(4)} = 24$;

4.3 Three Layer

Three-layer structure in prime number equal to 7 exist only in group 3,4 and 5. Fig. 3 shows an instance of the case. System capacity belong to the case is calculated as follow :

$$C_{\text{Three Layer}} = [(P_3^2\times 3)(P_3^2\times 3)S_{11-(2)}] + [C_2^3(P_3^2\times 2)(P_3^2\times 2)S_{10-(3)}] + [C_2^2(P_3^2\times 2)(P_3^2\times 2)S_{10-(2)}] + [C_2^4(P_3^2\times 1)(P_3^2\times 1)S_{9-(4)}] + [C_2^3(P_3^2\times 1)(P_3^2\times 1)S_{9-(3)}] = 10935$$

where $S_{11-(2)} = 5$;
$S_{10-(3)} = 4$;
$S_{10-(2)} = 3$;
$S_{9-(4)} = 3$;
$S_{9-(3)} = 4$;

4.4 Four Layer

Four-layer structure in prime number equal to 7 exist only in group 3 and 4. System capacity belong to the case is calculated as follow :

$$C_{\text{Four Layer}} = [(P_3^2\times 2)(P_3^2\times 2)(P_3^2\times 2)S_{10-(4)}] + [(P_3^2\times 1)(P_3^2\times 1)(P_3^2\times 1)S_{9-(3)}] + [C_3^4(P_3^2\times 1)(P_3^2\times 1)(P_3^2\times 1)S_{9-(4)}] = 34992$$

where $S_{10-(4)} = 4$;
$S_{9-(4)} = 3$;
$S_{9-(3)} = 4$;

4.5 Five Layer

Five-layer structure in prime number equal to 7 exist only in group 3. System capacity belong to the case is calculated as follow :

$$C_{\text{Five Layer}} = [(P_3^2\times 1)(P_3^2\times 1)(P_3^2\times 1)(P_3^2\times 1)S_{9-(4)}] = 19683$$

where $S_{9-(4)} = 3$;

4.6 Total Capacity

Total system capacity, as illustrate previously, can be obtain by sum up the result in section 4.1 ～ 4.4 :

$$C_{Total} = C_{Two\ Layer} + C_{Three\ Layer} + C_{Four\ Layer} + C_{Five\ Layer} + P_7^{\ 2}$$
$$= 1080 + 10935 + 34992 + 19683 + 49$$
$$= 66739$$

After simulation we proposed previously, we find out that only in the case of two-layer, we reach the capacity of 8,31 among theoretical capacity of 1080. The effective ratio is about 76.9%. Fig. 5 plot the results compare with those traditional scheme and theoretical capacity. There are still other cases : three-layer four-layer and five-layer, are needed to be verified to find out the real total capacity exactly of this prime code hierarchical decoder architecture.

5. CONCLUSION

The novel design using multi-hierarchical prime code architecture enables the implementation of higher capacity of decoder. The novel system can increase the decoder capacity from P^2 to $1362 \times P^2$ theoretically. Now we have already found out the capacity in the case of two-layer, and the ratio of success is 76.9%. There may be some failure groups among the theoretical capacity verified by simulations. Our future work is to utilize the simulation to verify all case in this multi-hierarchical decoder architecture and find out the real capacity of this system.

6. REFERENCES

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Modified Prime Sequence Codes for P = 3

Group	Code Sequences
0	C0,0=1 0 0 1 0 0 1 0 0
	C0,1=0 0 1 0 0 1 0 0 1
	C0,2=0 1 0 0 1 0 0 1 0
1	C1,0=1 0 0 0 1 0 0 0 1
	C1,1=0 1 0 0 0 1 1 0 0
	C1,2=0 0 1 1 0 0 0 1 0
2	C2,0=1 0 0 0 0 1 0 1 0
	C2,1=0 0 1 0 1 0 1 0 0
	C2,2=0 1 0 1 0 0 0 0 1

Table I. Modified Prime code sequence for P=3

Modified Prime Sequence Codes for P = 7

Group	Code Sequences
0	C0,0=1000000 1000000 1000000 1000000 1000000 1000000 1000000
	C0,1=0000001 0000001 0000001 0000001 0000001 0000001 0000001
	C0,2=0000010 0000010 0000010 0000010 0000010 0000010 0000010
	C0,3=0000100 0000100 0000100 0000100 0000100 0000100 0000100
	C0,4=0001000 0001000 0001000 0001000 0001000 0001000 0001000
	C0,5=0010000 0010000 0010000 0010000 0010000 0010000 0010000
	C0,6=0100000 0100000 0100000 0100000 0100000 0100000 0100000
1	C1,0=1000000 0100000 0010000 0001000 0000100 0000010 0000001
	C1,1=0100000 0010000 0001000 0000100 0000010 0000001 1000000
	C1,2=0010000 0001000 0000100 0000010 0000001 1000000 0100000
	C1,3=0001000 0000100 0000010 0000001 1000000 0100000 0010000
	C1,4=0000100 0000010 0000001 1000000 0100000 0010000 0001000
	C1,5=0000010 0000001 1000000 0100000 0010000 0001000 0000100
	C1,6=0000001 1000000 0100000 0010000 0001000 0000100 0000010
2	C2,0=1000000 0010000 0000100 0000001 0100000 0001000 0000010
	C2,1=0010000 0000100 0000001 0100000 0001000 0000010 0100000
	C2,2=0000100 0000001 0100000 0001000 0000010 0100000 0001000
	C2,3=0000001 0100000 0001000 0000010 0100000 0001000 0000010
	C2,4=0100000 0001000 0000010 0100000 0001000 0000010 0100000
	C2,5=0001000 0000010 0100000 0001000 0000010 0100000 0001000
	C2,6=0000010 0100000 0001000 0000010 0100000 0001000 0000010
3	C3,0=1000000 0001000 0000001 0010000 0000010 0100000 0000100
	C3,1=0001000 0000001 0010000 0000010 0100000 0000100 1000000
	C3,2=0000001 0010000 0000010 0100000 0000100 1000000 0001000
	C3,3=0010000 0000010 0100000 0000100 1000000 0001000 0000001
	C3,4=0000010 0100000 0000100 1000000 0001000 0000001 0010000
	C3,5=0100000 0000100 1000000 0001000 0000001 0010000 0000010
	C3,6=0000100 1000000 0001000 0000001 0010000 0000010 0100000
4	C4,0=1000000 0000100 0100000 0000010 0010000 0000001 0001000
	C4,1=0000100 0100000 0000010 0010000 0000001 0001000 1000000
	C4,2=0100000 0000010 0010000 0000001 0001000 1000000 0000100
	C4,3=0000010 0010000 0000001 0001000 1000000 0000100 0100000
	C4,4=0010000 0000001 0001000 1000000 0000100 0100000 0000010
	C4,5=0000001 0001000 1000000 0000100 0100000 0000010 0010000
	C4,6=0001000 1000000 0000100 0100000 0000010 0010000 0000001
5	C5,0=1000000 0000010 0001000 0100000 0000001 0000100 0010000
	C5,1=0000010 0001000 0100000 0000001 00C0100 0010000 1000000
	C5,2=0001000 0100000 0000001 0000100 0010000 1000000 0000010
	C5,3=0100000 0000001 0000100 0010000 1000000 0000010 0001000
	C5,4=0000001 0000100 0010000 1000000 0000010 0001000 0100000
	C5,5=0000100 0010000 1000000 0000010 0001000 0100000 0000001
	C5,6=0010000 1000000 0000010 0001000 0100000 0000001 0000100
6	C6,0=1000000 0000001 0000010 0000100 0001000 0010000 0100000
	C6,1=0000001 0000010 0000100 0001000 0010000 0100000 1000000
	C6,2=0000010 0000100 0001000 0010000 0100000 1000000 0000001
	C6,3=0000100 0001000 0010000 0100000 1000000 0000001 0000010
	C6,4=0001000 0010000 0100000 1000000 0000001 0000010 0000100
	C6,5=0010000 0100000 1000000 0000001 0000010 0000100 0001000
	C0,6=0100000 1000000 0000001 0000010 0000100 0001000 0010000

Table II Modified Prime code sequence for P=7

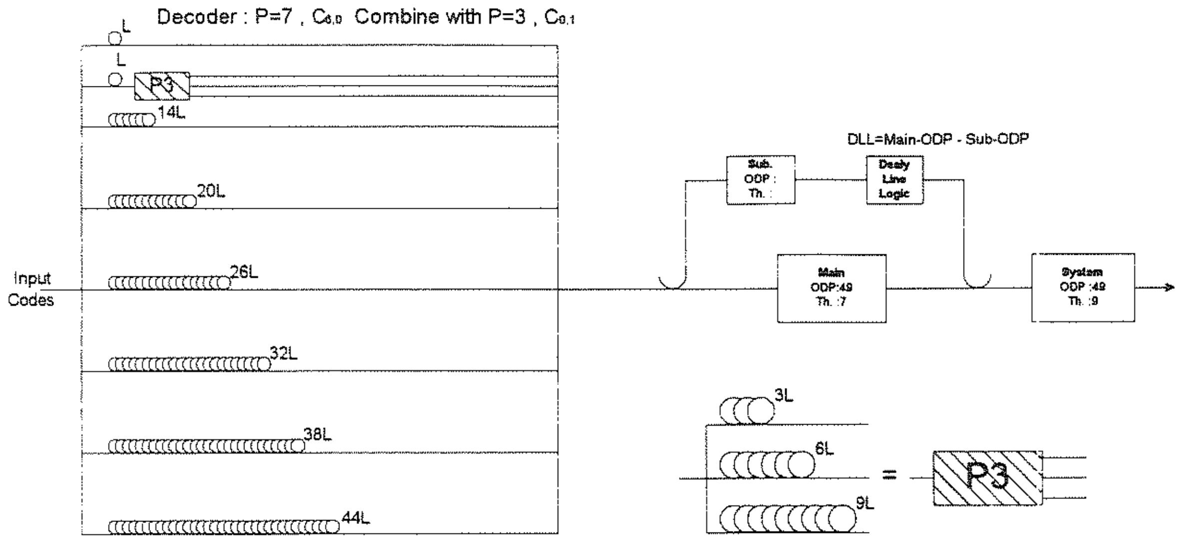


Fig. 1 Multi-Hierarchical Prime Code Structures with Delay Line Logic.

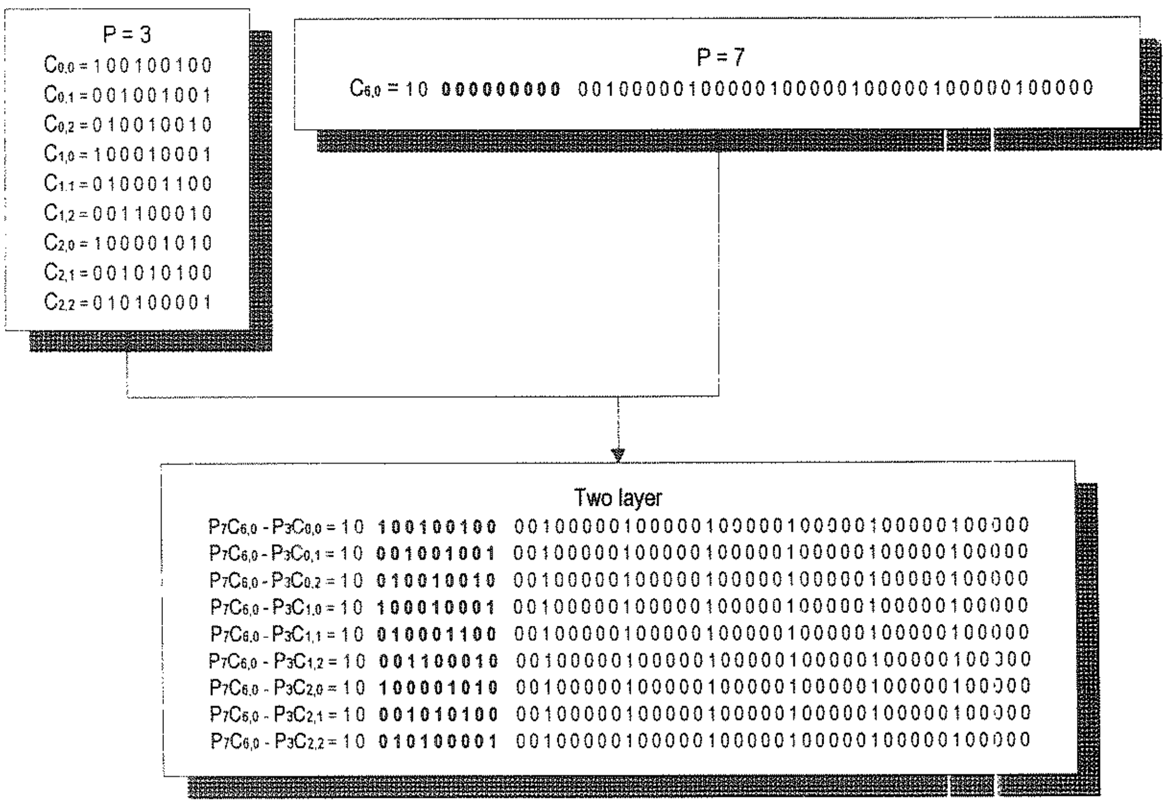


Fig. 2 Combination from Different P values of Modified Prime Codes ($P_L = P_7 = 7$ and $P_S = P_3 = 3$) to form a two-layer structure → Multi-Hierarchical Modified Prime Codes.

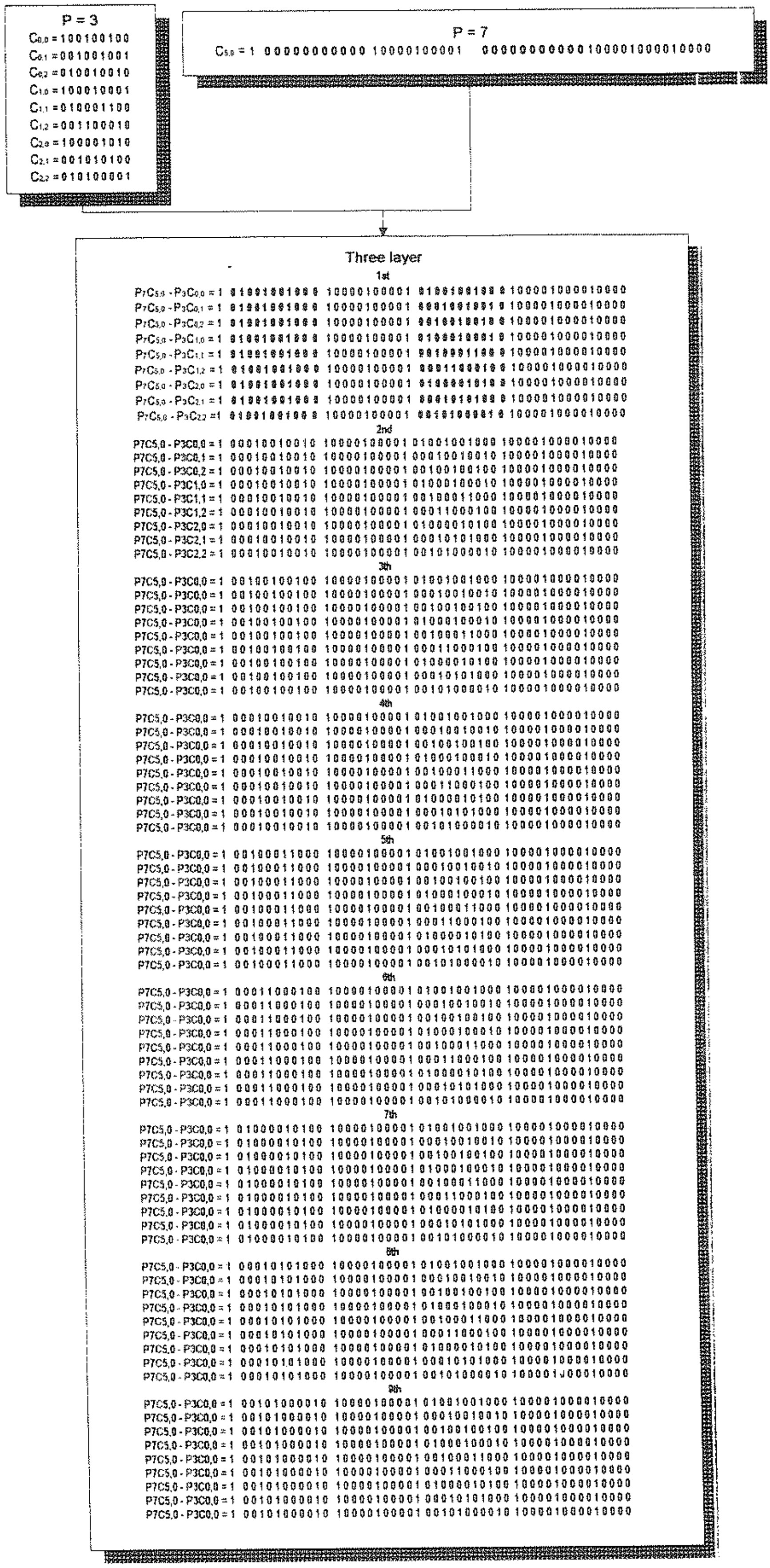


Fig. 3 Combination from Different P values of Modified Prime Codes ($P_L = P_7 = 7$ and $P_S = P_3 = 3$) to form a three-layer structure → Multi-Hierarchical Modified Prime Codes.

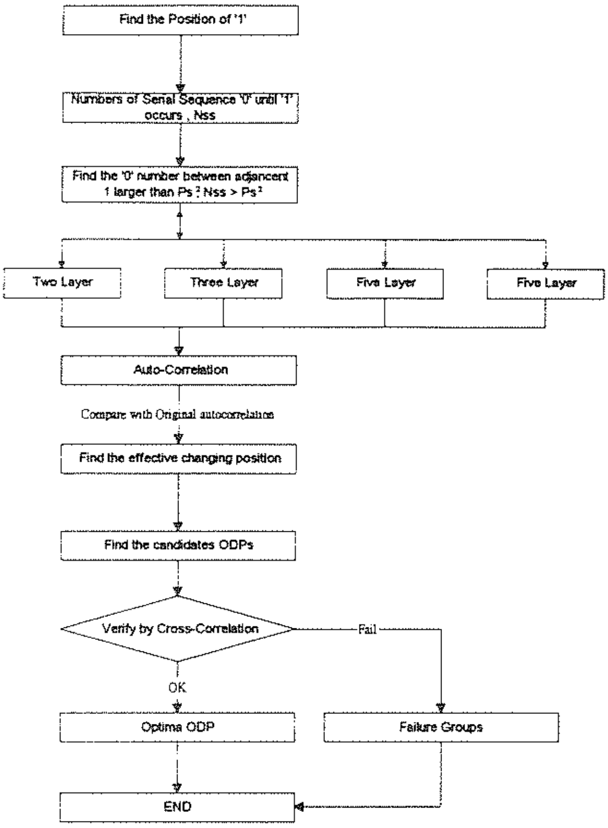


Table III. Algorithm for designing the multi-hierarchical prime code architecture and find out the optimal decision positions (ODPs) for the decoder.

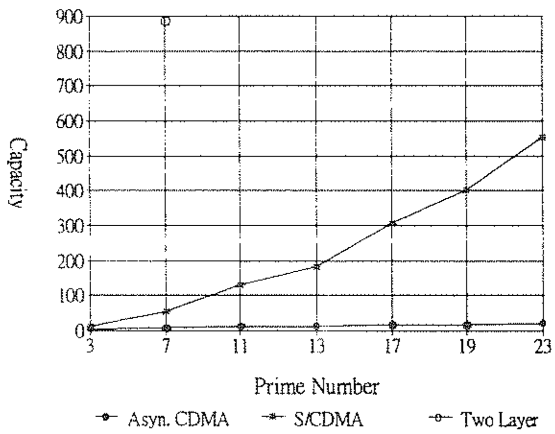
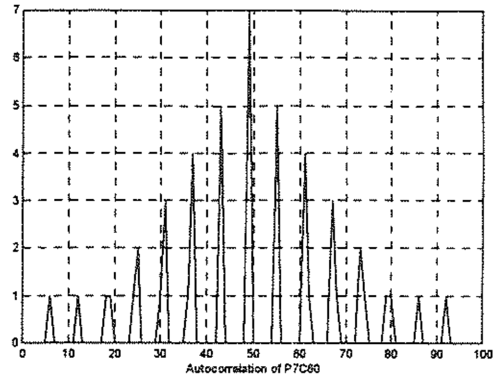
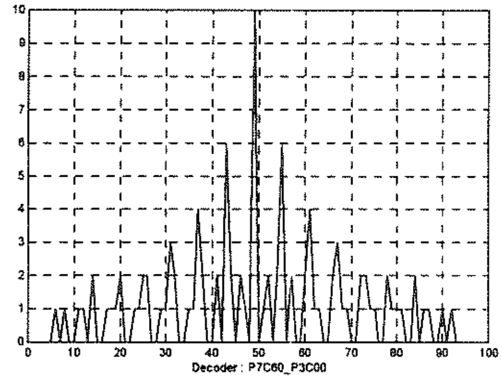


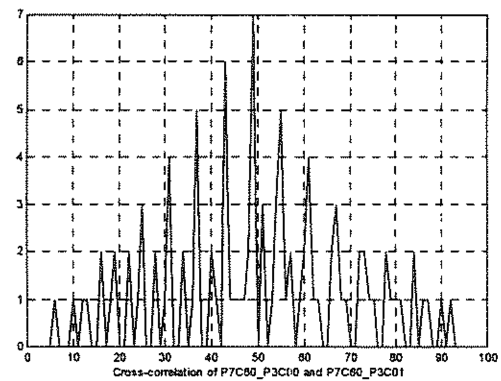
Fig. 5 A comparison in capacity with various scheme.



(a)



(b)



(c)

Fig. 4 (a) A plot of autocorrelation function of P=7,$C_{6,0}$ before combination. (b) A plot of autocorrelation function of P=7,$C_{6,0}$-P=3,$C_{0,0}$ after combination. (c) A plot of cross-correlation function of P=7, $C_{6,0}$ - P=3, $C_{0,0}$ and P=7, $C_{6,0}$ - P=3, $C_{0,1}$ .After simulation we find out that at bit 14,20,26,32, the amplitude in (b) are greater than (c), thus we finish one example of our decoder design.